In the Claims:

1. (Currently Amended) A memory controller ~~An apparatus~~, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache ~~associated with~~ located on a memory module, the memory controller coupled to the memory module via a memory bus, the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module .

A1

2. Cancelled

3. (Currently Amended) The memory controller ~~The apparatus~~ of claim 2, the command sequencer and serializer to deliver a writeback command to the data cache associated with the memory module, the writeback command to cause the previous line of data stored in the eviction buffer to be written out to a memory module memory device.

4. (Currently Amended) The memory controller ~~The apparatus~~ of claim 3, the writeback command including way information and bank address information.

5. (Currently Amended) A memory module ~~An apparatus~~, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller ~~component~~ over a memory bus, the memory controller ~~component~~ including an array of tag address storage locations, the memory controller ~~writing~~ to write a current line of data to the data cache, the memory controller to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module.

6. (Currently Amended) The memory module ~~The apparatus~~ of claim 5, the memory controller to further instruct ~~instructing~~ the data cache to evict a previous line of data from the data cache into an eviction buffer.

7. (Currently Amended) The memory module ~~The apparatus~~ of claim 6, the memory module to receive ~~controller to deliver~~ a writeback command ~~to the data cache~~, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device.

8. (Currently Amended) The memory module ~~The apparatus~~ of claim 7, the writeback command including way information and bank address information.

9. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag

address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer.

A1

10. Cancelled

11. (Original) The system of claim 10, the memory controller to deliver a writeback command to the data cache, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device.

12. (Original) The system of claim 11, the writeback command including way information and bank address information.

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13. Cancelled

14. Cancelled

15. Cancelled